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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,375	01/31/2001	John F. McEntee	10004032-1	7821

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AGILENT TECHNOLOGIES
Legal Department, 51U-PD
Intellectual Property Administration
P.O. Box 58043
Santa Clara, CA 95052-8043

EXAMINER

HANDY, DWAYNE K

ART UNIT	PAPER NUMBER
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1743

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/775,375

Applicant(s)

MCENTEE ET AL.

Examiner

Dwayne K. Handy

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21, 32 and 33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-21, 32 and 33 is/are rejected.
- 7) ☒ Claim(s) 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-8, 10-21, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Besemer et al. (6,140,044) in view of Juntunen et al. (5,325,624). Besemer teaches an apparatus for packaging a probe array. The probe array is described in general in column 5. It is comprised of a wafer or chip that may be comprised of a wide variety of materials. The use of an array of DNA on silicon materials is disclosed in column 6. Besemer teaches a wide variety of chip holders for use with the chip array, as well as how to load them, in columns 13-15. All of the chip holder embodiments involve the placement of the chip into a housing that holds the chip (Figures 16A-24). The chip may be sealed into the housing through the use of a cover (2770), which may take the form of an adhesive film (column 15, lines 37-48). As shown in the various Figures cited, the chip may be placed in the housing while leaving room both above and under the chip between the chip and another surface (cover film or bottom of the housing). Besemer teaches fluid retention and delivery to the chip while in the housing via duck billed check valves (septa) in column 14, lines 49-57. Besemer does NOT teach multiple microarrays in a pocket strip having a number of pockets. Besemer teaches a single microarray chip held in a single housing.

Juntunen teaches a carrier tape and cover strip for storing electronic components. The carrier tape is best shown in Figures 3-6. The carrier tape (100) includes pockets (112) for holding components covered by a cover strip (120). The cover strip is bonded to the edges (104, 106) of the carrier strip by heat or pressure (col. 5, lines 40-55) to form sealed chambers containing the electrical components. The

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carrier includes holes (108, 110) for mating with automated equipment to advance the strip. It would have been obvious to one of ordinary skill in the art to combine the carrier strip teaching from Juntunen with the holder of Besemer. One would use the carrier strip from Juntunen in order to provide the individual chips of Besemer in sealed chambers while also providing the chips in bulk.

Response to Arguments

4. Applicant's arguments, filed 10/25/05, with respect to the rejection(s) of claim(s) under Besemer and Runyon have been fully considered and are persuasive. The Examiner agrees with Applicant's assertion that Runyon does not teach a carrier strip having sealed chambers. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Besemer and Juntunen. The new reference, Juntunen, teaches a carrier strip having components in sealed chambers.

While the Examiner has removed the previous rejection involving Runyon, the Examiner wishes to comment on Applicant's arguments submitted 10/25/05 involving the combination of references. Applicant has argued that one would not be motivated to combine a carrier strip having electronic components with the chip holder of Besemer. The Examiner respectfully disagrees. Besemer teaches a single chip in a sealed holder or package. Besemer teaches that their chip may be made from "Si, Ge, GaAs, GaP, SiO₂, SiN₄, modified silicon..." (col. 5, lines 55-56). These are materials are commonly used in making electronic components. Juntunen teaches the packaging of electronic

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components in sealed chambers of a carrier strip. The large number of pockets allows for a continuous supply of components (col. 1, lines 40-44). The pockets are sealed to protect the components (col. 1, lines 48-51). Given these teachings, the Examiner believes that one of ordinary skill in the art would be motivated to use the carrier strip from Juntunen with the chip package of Besemer without using the hindsight Applicant suggests is necessary. One would use the carrier strip to provide large numbers of the chips in an automated fashion.

Allowable Subject Matter

5. Claim 9 remains objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schenz et al. (5,361,901), Tidemann et al. (5,526,935) and Bird (5,648,136) teach carrier strips.


7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwayne K. Handy whose telephone number is (571)-272-1259. The examiner can normally be reached on M-F 8:00-4:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jill Warden can be reached on (571)-272-1267. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKH
January 9, 2006


Jill Warden
Supervisory Patent Examiner
Technology Center 1700